

REMARKS

Claims pending in the instant application are numbered 1-7 and 20-27. Claims 1-7 and 20-27 are rejected.

The Applicant respectfully requests reconsideration of the present application in view of the amendments and the following remarks.

35 U.S.C. § 102 and § 103 Rejections

Claims 1, 3-7, 20, 22-24 and 27 are rejected under 35 U.S.C. § 102(b) as being anticipated by Gnadinger U.S. 5,229,647.

Claims 2, 21 and 25 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Gnadinger, in view of Hsuan, U.S. 6,429,509.

Claim 1 as presently amended expressly recites (emphasis added):

a dielectric layer positioned on top of a semiconductor support layer;

a via passing through the dielectric layer and the semiconductor support layer,

wherein a first end of the via is positioned in the dielectric layer and a second end of the via is positioned in the semiconductor support layer, wherein a first diameter of the first end is greater than a second diameter of the second end; and

a contact positioned on top of the dielectric layer, the contact coupled to the first end of the via, wherein the contact to be coupled to a device of the die.

The Examiner's attention is directed to at least page 6, lines 8-9, of the specification as originally filed.

Gnadinger is directed to stacked wafers. In Figure 6, Gnadinger discloses an oxide layer 24 proximate to a wafer 10. A through-hole 21 passes through wafer 10. The narrow end of through-hole 21 is at pad 40. The wide end of through-hole 21 is at pad 43.

However, pad 43 is not coupled to a device of wafer 10. Pad 43 is used to couple the through-hole 21 to another, distinct wafer 10 (see wafer stacking in Figure 4). Thus, Gnadinger fails to disclose "wherein a first diameter of the first end is greater than a second diameter of the second end ...the contact coupled to the first end of the via, wherein the contact to be coupled to a device of the die" as expressly claimed by the Applicant.

Hsuan is directed to an interconnect structure of an integrated circuit. A top interconnect node 210 is located on a top surface of die 230, where the top interconnect node 210 is connected to electronic circuits formed in and on die 230 (such as in active layer 243) (col. 4, lines 64-67; col. 6, lines 49-64). Bottom interconnect node 215 serves as a primary interconnect for I/O signals for inter-chip interconnects such as power and ground supply (col. 5, lines 45-62).

In Figure 2D of Hsuan, conductive layer 217 has a smaller diameter than conductive layer 216. Layer 217 is connected to top interconnect 210 that is connected to a device of die 230. Thus, Hsuan fails to disclose "wherein a first diameter of the first end is greater than a second diameter of the second end ...the contact coupled to the first end of the via, wherein the contact to be coupled to a device of the die" as expressly claimed by the Applicant.

Therefore, Gnadinger and Hsuan, whether taken singularly or in combination, fail to disclose, teach, or fairly suggest at least one of the expressly recited limitations of claim 1. Accordingly, claim 1 is not anticipated nor rendered obvious by the cited references. Independent claims 20 and 24 distinguish for at least the same reasons as claim 1. Claims 2-5, 7, 21-23 and 25-27 are dependent claims and distinguish for at least the same reasons as their independent base claims in addition to adding further limitations of their own. Therefore, the Applicant respectfully requests that the instant § 102 and § 103 rejections be withdrawn.

Conclusion

The Applicant submits that in view of the remarks and amendments set forth herein, all pending claims are in condition for allowance. Therefore, the Applicant respectfully requests the Examiner to issue a Notice of Allowance in this case.

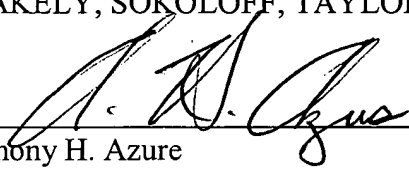
Charge Deposit Account

Please charge our Deposit Account No. 02-2666 for any additional fee(s) that may be due in this matter, and please credit the same deposit account for any overpayment.

Respectfully submitted,

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Date: July 7, 2005



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